IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kevin J. Ryan	Examiner: James Peikari
Serial No.:	09/434,082	Group Art Unit: 2186
Filed:	November 5, 1999	Docket: 303.306US2
Title:	PIPELINED PACKET-ORIENTED MEMORY SYSTEM HAVING A UNIDIRECTIONAL COMMAND AND ADDRESS BUS AND A BIDIRECTIONAL DATA BUS	

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on March 27, 2001. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. Specific amendments to individual claims are detailed in the following marked up set of claims.

Please amend the claims as follows:

5. (Amended) A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

[a)] a plurality M of memory devices wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

[b)] a command buffer [register] connected between the command and address bus and the plurality of memory devices, the command buffer [register] receiving and latching